REMARKS

In the final Office Action mailed 30 April 2007, the Examiner maintained and reiterated his rejection of claims 1-2, 4-6, 11-15, 17, 20-21, 23-25 and 28-30 under 35 U.S.C. §102(e); of claims 3 and 22 under 35 U.S.C. §103(a); of claims 7-8, 18-19 and 31-32 under 35 U.S.C. §103(a); of claims 9 and 26 under 35 U.S.C. §103(a); of claims 10 and 27 under 35 U.S.C. §103(a); and of claim 16 under 35 U.S.C. §103(a). Claims 1-32 remain pending.

Rejection of Claims 1-2, 4-6, 11-15, 17, 20-21, 23-25 and 28-30 under 35 U.S.C. §102(e)

Applicant requests reconsideration of the rejection because the Examiner has mischaracterized the Ikeda reference in asserting that Ikeda discloses memory storing instructions for a "configuration load function" and a "configuration function" for configuring the FPGA, as explained in more detail below.

Claim 1 of the present invention is reproduced below:

> 1. An integrated circuit, comprising:
> an input port by which data is received from a source external to the integrated circuit;
> a configurable logic array having a programmable configuration defined by configuration data stored in electrically programmable configuration points within the configurable logic array;
> memory storing instructions for a mission function for the integrated circuit, storing instructions for a configuration load function used to receive configuration data via said input port, and storing instructions for a configuration function used to transfer the configuration data to the programmable configuration points within the configurable logic array; and
> a processor coupled to the memory which fetches and executes said instructions from the memory.

The Examiner asserts that paragraph [0052] and Figure 1 of Ikeda disclose the claimed "configuration load function" and "configuration function" of claim 1 for configuring an FPGA (See Office Action, Page 9 and 10). Paragraph [0052] of Ikeda is reproduced below:

> **[0052]** The matrix **20** and the FPGA **14** are connected by a data bus **21**. Data is supplied from the matrix **20** to the FPGA **14**, processing is performed, and the result is returned to the matrix **20**. The matrix **20** is connected to the bus control unit **15** by a load bus **22** and a store bus **23**, and exchanges data with an external data bus of the system LSI **10**. Accordingly, data can be inputted into the matrix **20** from an external DRAM **2** or another external device, and the result of such data being processed by the matrix **20** can be outputted back to the external device. The processor **11** is also capable of inputting and outputting data to and from an external device via a combination of a data bus **11***a* and the bus control unit **15**. If the processor **11** is constructed with an internal code RAM or ROM, the execution program (object program) **3** of the processor **11** can be stored in advance in the processor **11**. The execution program **3** can also be supplied from outside the LSI **10** via the bus **11***a*.

The Examiner has mistakenly characterized the "data" supplied from the matrix to the FPGA in paragraph [0052] as "configuration data" for the FPGA. In fact, as can be seen in lines 2-4 of paragraph [0052], the "data" is working data that is supplied from the matrix 20, processed by the FPGA, and that processed result in then returned to the matrix 20. This processing of working data by the FPGA is described throughout Ikeda including in Figure 11 and paragraph [0077] in which Ikeda states that "processing in the matrix 20 can be continuously performed by supplying input data to the offchip FPGA 14 and returning the data to the matrix 20 after processing in the FPGA 14." Furthermore, in a search of Ikeda no mention of configuring the FPGA is described.

The Examiner appears to rely on this mistaken characterization of the "data" in order to come to the conclusion that memory must store instructions for a configuration load function used to configure the FPGA. The Examiner admits that Ikeda does not specifically recite that the memory stores instructions for a configuration load function and instead concludes that instructions must be stored in the memory "since the matrix is controlled by the instructions/commands from the processor which executes instructions stored in memory". (See Office Action, page 9-10). Ikeda does disclose that instructions are incorporated directly into the execution program stored in memory and that the processor controls the configuration of the

matrix according to the instructions in the execution program (See, Ikeda paragraph [0111]). However, Ikeda does not disclose configuring the FPGA in any such manner. Ikeda actually discloses that an advantage of his invention of configuring a matrix instead of programming the FPGA is "[w]ith this integrated circuit device, there is no need to change all the connections at the transistor level as is the case with an FPGA, so that the hardware can be reconfigured in a short time." (Ikeda, paragraph [0005]).

Therefore, the Examiner has mischaracterized Ikeda since Ikeda does not disclose memory storing instructions for a "configuration load function" and a "configuration function" for configuring the FPGA, and in fact describes an advantage of Ikeda's invention is that a matrix is configured instead of the FPGA.

Accordingly, the Examiners rejection of claim 1 is incorrect and claim 1 is patentably distinct from Ikeda.

Claims 2, 4-6, 11-15, and 17 depend from claim 1, and are patentable for at least the same reasons as claim 1.

In the rejection of independent claim 20, the Examiner states "As per claims 20-21, 23-25, and 28-30, see arguments with respect to the rejection of claims 1-2, 4-6 and 11-13, respectively. Claims 20-21, 23-25, and 28-30 are also rejected based on the same rationale as the rejection of claims 1-2, 4-6 and 11-13, respectively." (Office Action, pages 4-5).

The Examiner has made the same mischaracterization of Ikeda in the rejection of claim 20 as in claim 1, and therefore claim 18 is patentable for at least the same reasons as claim 1.

Claims 21, 23-25, and 28 depend from claim 20, and are patentable for at least the same reasons.

Accordingly, reconsideration of the rejection of claims 1-2, 4-6, 11-15, 17, 20-21, 23-25 and 28-30 is respectfully requested.

Rejection of Claims 3 and 22 under 35 U.S.C. §103(a)

Claim 3 depends from claim 1, and claim 22 depends from claim 20, and therefore such claims are patentable for at least the reasons discussed above and because of the unique combinations recited.

Accordingly, reconsideration of the rejection of claims 3 and 22 is respectfully requested.

Rejection of Claims 7-8, 18-19 and 31-32 under 35 U.S.C. §103(a)

The Examiner states that independent claim 18 is "rejected based on the same rationale as the rejection of claim 8." (Office Action, page 6). Claim 8 depends from claim 1 and both claim 1 and claim 18 include a "configuration load function".

The Examiner has made the same mischaracterization of Ikeda in the rejection of claim 18 as in claim 1, and therefore claim 18 is patentable for at least the same reasons as claim 1.

Claim 19 depends from claim 18 and is patentable for at least the same reasons.

Accordingly, reconsideration of the rejection of claims 7-8, 18-19 and 31-32 is respectfully requested.

Rejection of Claims 9 and 26 under 35 U.S.C. §103(a)

Claim 9 depends from claim 1, and claim 26 depends from claim 20, and therefore claims 9 and 26 are patentable for at least the reasons discussed above and because of the unique combinations recited.

Accordingly, reconsideration of the rejection of claims 9 and 26 as is respectfully requested.

Rejection of Claims 10 and 27 under 35 U.S.C. §103(a)

Claim 10 depends from claim 1, and claim 27 depends from claim 20, and therefore such claims are patentable for at least the reasons discussed above and because of the unique combinations recited.

Accordingly, reconsideration of the rejection of claims 10 and 27 is respectfully requested.

Rejection of Claim 16 under 35 U.S.C. §103(a)

Claim 16 depends from claim 1, and therefore is patentable for at least the reasons discussed above and because of the unique combination recited.

Accordingly, reconsideration of the rejection of claim 16 is respectfully requested.

CONCLUSION

It is respectfully submitted that this application is now in condition for allowance, and such action is requested.

The Commissioner is hereby authorized to charge any fee determined to be due in connection with this communication, or credit any overpayment, to our Deposit Account No. 50-0869 (MXIC 1520-1).

Respectfully submitted,

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